REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-3, 6-8 and 19-22 are pending in this case. Claims 21 and 21 are added herein and claims 4, 5, 17, and 18 are cancelled herein.

The Examiner objected to claims 4 and 5 as being depended upon a rejected base claim, but that would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 4 is rewritten as claim 21 and claim 5 is rewritten as claim 22 including all the limitations of the base claim (claim 1) and the intervening claim (claim 3). Allowance of claims 21 and 22 is requested.

The Examiner objected to the drawings as not showing every feature of the claims. Specifically, the Examiner argued that the drawings do not show the first plurality of conductively filled vias extending form the upper interconnect layer to the lower interconnect layer. Fig. 1 shows a representative partial cross-section of a semiconductor device. While only a single via extending from the upper interconnect layer to the lower interconnect layer is shown for simplicity, it would be apparent those of ordinary skill in the art that many such vias would be included in the device. Multiple vias between metal interconnect levels are commonplace. In fact, the specification refers to plural "vias 95 to the lower interconnect layer 40" on page 8, lines 4-5. Accordingly, Applicant respectfully requests that the objection be withdrawn.

The Examiner rejected claims 18 and 20 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. As noted above, the specification does recite plural "vias 95 to the lower interconnect layer 40" on page 8, lines 4-5. Accordingly, Applicant requests that the rejection be withdrawn.

The Examiner rejected claims 1, 17 and 19 under 35 U.S.C. 102(b) as b ing anticipated by Keil et al. (U.S. Patent 5,541,442). Claim 17 is cancelled.

Applicant respectfully submits that claim 1 is unanticipated by Keil as there is no disclosure or suggestion in Keil of a thin film resistor embedded within a multi-level dielectric layer between a lower metal interconnect layer and an upper metal interconnect layer, wherein the thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer. Keil teaches a resistor 38 formed at the first metal interconnect level (35, 36). A second metal interconnect level 46 is formed above the resistor 38. Resistor 38 is not, however, formed between a lower metal interconnect layer and an upper metal interconnect layer. Instead, it is formed at the lower metal interconnect level 35, 36. Contacts 30 and 34 are not a metal interconnect level as that term is used in the art. They are contacts from the first metal interconnect level 35, 36 to either the substrate or the gate electrode. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Keil.

Applicant respectfully submits that claim 19 is unanticipated by Keil as there is no disclosure or suggestion in Keil of a second metal interconnect layer located over a first metal interconnect layer, there being no additional metal interconnect layers between the first and second metal interconnect layers, a multi-level dielectric layer located between the first metal interconnect layer and the second metal interconnect layer, and a thin film resistor embedded within the multi-level dielectric layer such that the multi-level dielectric layer separates the thin film resistor from both the first metal interconnect layer and the second metal interconnect layer. As discussed above, Keil teaches forming the resistor 38 at the first interconnect layer 35, 36. If contacts 30 and 34 where considered a metal interconnect layer, then there is an additional metal interconnect layer 35,36 between contacts 30,34 and metal interconnect layer 46, in contrast to the claim requirements. Accordingly, Applicant respectfully submits that claim 19 is unanticipated by Keil.

The Examiner rejected claims 1-3, 17 and 19 under 35 U.S.C. 102(e) as being anticipated by Ishikawa et al. (U.S. Patent 5,751,050).

Applicant respectfully submits that claim 1 is unanticipated by Ishikawa as there is no disclosure or suggestion in Ishikawa of a thin film resistor embedded within a multi-level dielectric layer between a lower metal interconnect layer and an upper metal interconnect layer, wherein the thin film resistor comprises a resistor layer that is physically separated, in its entirety, in a vertical direction from any metal interconnect layer. Ishikawa teaches a resistor formed below the first wiring layer 82. Resistor 73 is not located between a lower and an upper metal interconnect layer as required by the claim. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Ishikawa.

Applicant respectfully submits that claim 2 is further unanticipated by Ishikawa as there is no disclosure or suggestion in the reference of a first via extending from the upper metal interconnect layer to the lower interconnect layer and a second via extending from the upper metal layer to the thin film resistor. Second metal layer 80 extends from wiring layer 82 to the resistor 73 similar to the claimed second via, but there is no first via extending from an upper metal interconnect to a lower metal interconnect. A contact/via 81 extends from the first wiring layer to the source/drain region 75, but it does not extend between an upper and lower metal interconnect layer. If wiring layer 82 is the upper metal interconnect layer, then there is no lower metal interconnect layer in Ishikawa. Accordingly, Applicant respectfully submits that claim 2 is further unanticipated by Ishikawa.

Applicant respectfully submits that claim 19 is unanticipated by Ishikawa as there is no disclosure or suggestion in Ishikawa of a second metal interconnect layer located over a first metal interconnect layer, there being no additional metal interconnect layers between the first and second metal interconnect layers, a multi-level dielectric layer located between the first metal interconnect layer and the second metal interconnect layer, and a thin film resistor embedded within the multi-level dielectric layer such that

the multi-lev l dielectric layer separates the thin film resistor from both th first metal interconnect layer and the second metal interconnect layer. Wiring layer 82 of Ishikawa is the first metal interconnect layer and only metal interconnect layer shown in FIG. 8 of Ishikawa. The resistor 73 of Ishikawa is not located between a first and second metal interconnect layer as required by the claim. Accordingly, Applicant respectfully submits that claim 19 is unanticipated by Ishikawa.

The Examiner rejected claims 17 and 18 under 35 U.S.C. 102(e) as being anticipated by Saia et al. (U.S. Patent 5,874,770). Claims 17 and 18 are cancelled.

The Examiner rejected claims 6-8 under 35 U.S.C.§ 103(a) as being unpatentable over Ishikawa as applied to claim 1 above, and further in view of Redford et al. (U.S. Patent 6,081,014).

Applicant respectfully submits that claims 6-8 are patentable over Ishikawa in view of Redford for the same reasons discussed above relative to claim 1 from which these claims depend.

The other references cited by the Examiner have been reviewed, but are not felt to come within the scope of the claims as amended.

In light of the above, Applicant resp ctfully requests withdrawal of the Examiner's rejections and allowance of claims 1-3, 6-8 and 19-22. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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